

## Phase Modulated PWM Topology with the ML4818

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### INTRODUCTION

One of the biggest goals in power supply design is to get the maximum amount of output power while maximizing efficiency and minimizing both the cost and size of the respective power supplies. There are many conflicting parameters in trying to do so. For example, let's examine how the size of a power supply is a strong function of the size of the passive storage elements. It is well known that the size of inductors and capacitors greatly depends on the operating frequency. The higher the frequency the smaller the inductors and capacitors necessary. Increasing the operating frequency is one thing, implementing it is another. It is also a well known fact that increased operating frequencies result in lower efficiencies in PWM controlled switched mode power supplies.

Increasing the frequency of PWM controlled power supplies was one solution in the reduction of the passive elements. That posed some limitations due to the nature of operation. Simultaneous conduction of high currents in the presence of high voltage during turn-on and turn-off times at high frequencies resulted in high switching losses. Thus violating one of the most important parameters of the switching power supply design that is the efficiencies were now lower than in lower frequency operation.

This application note will introduce the "Phase Modulated PWM Topology" that overcomes many of the shortcomings of conventional PWM topologies at high operating frequencies.

### LOSSES IN SWITCHING POWER SUPPLIES

The typical losses in switching power supplies can be divided in two classes conduction losses and switching losses. The most common switching element used in modern switching power supplies is the power MOSFET. This device when enhanced for conduction has a finite channel resistance named  $R_{DS(ON)}$ . When current passes through this device conduction losses result which are proportional to:

$$P_C = I_{DS(RMS)}^2 R_{DS(ON)}$$

In addition to the conduction losses, due to the switching action of the device in the presence of high currents and high voltages, there are also switching losses. These losses can be further subdivided in turn-on, turn-off and capacitive discharge losses. Figure 1 shows how turn-off losses can result during switching in a simplified way.

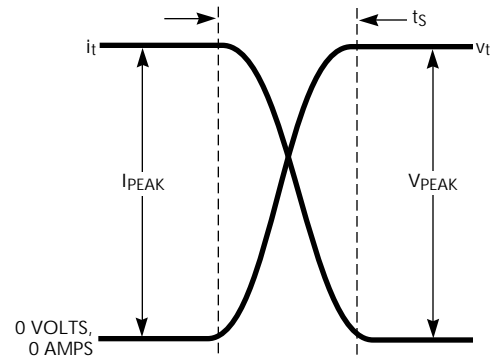


Figure 1. Waveforms in the switching element in a switching power supply during turn-off, assuming linear rise and fall.

The energy in turn-off instance can be found by integrating the product of the voltage and current waveforms over the complete switching interval i.e.,

$$W_{tOFF} = \int_0^{t_s} v_t i_t dt$$

Assuming linear waveforms and symmetry the above integral can be simplified to the following:

$$W_{tOFF} = \frac{1}{2} I_{PEAK} V_{PEAK} t_s$$

The total power lost therefore can be found by multiplying the above with the repetition rate, that is the switching frequency hence

$$P_{OFF} = \frac{1}{2} I_{PEAK} V_{PEAK} t_s f$$

To give an example suppose that the power switch switches 10 amps at 380 volts for 50nsec at 100KHz. The resulting power loss due to just this event would be 9.5 Watts. At 200KHz it would be 19 Watts and so on. This power loss must be dissipated by the switching element and poses a problem for the adequate removal of the generated heat. One can appreciate the losses at even higher frequencies.

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Turn-on switching losses result in a similar manner. Assuming again symmetry the turn-on losses can be found by integrating the current and voltage waveforms over the switching interval.

$$P_{ON} = \frac{1}{2} I_{PEAK} V_{PEAK} t_s f$$

We are going to see later that the switching event is more complicated than what is depicted above due to the presence of parasitic inductive and capacitive components such as leakage and lead inductances and drain source capacitances.

To reduce the switching losses several methods were used such as dissipative and non dissipative snubbers. As the name implies dissipative snubbers dissipate their energy as heat, whereas the non-dissipative snubbers return their energy back to the input line, thus tending to be more efficient. In any case even with the use of non dissipative snubbers there remain problems that limit the maximum operating frequency.

Several respected institutions along with many manufacturers tried to find a way around the above problems. This resulted in the proliferation of several new power supply topologies with each one claiming to be the solution for operation at high frequencies.

Resonant power supplies thought to be a possible solution had their own share of problems. Although not a new technology they found a home in some applications. They were never really widely accepted by the industry. Part of the reason was the absence of analytical tools for the analysis and design and suitable controllers. Thanks to the efforts of many people they are better understood today but most of the manufacturers are still reluctant to put products on the market based on this technology.

Resonant power supplies encompass a wide range of topologies and they can be subdivided into three major subclasses. These are as follows:

- 1) Current resonant or zero current switching ZCS.
  - 2) Voltage resonant or zero voltage switching ZVS.
- and
- 3) Multi-resonant, in the majority of which both the current and voltage is resonant.

It is beyond the scope of this application note to give an exhaustive explanation for each type of the resonant conversion techniques. For more information, the interested reader can draw on the vast amount of technical papers published over the last few years. It suffices to say that among the resonant conversion techniques one that is of particular interest for high frequency operation is the zero voltage switching, or ZVS.

Switches such as power MOSFETs have a drain-source capacitance of several hundred picofarads. When this capacitance charges and discharges, energy is lost that results in power loss. Figure 2, shows a typical power switch configuration.

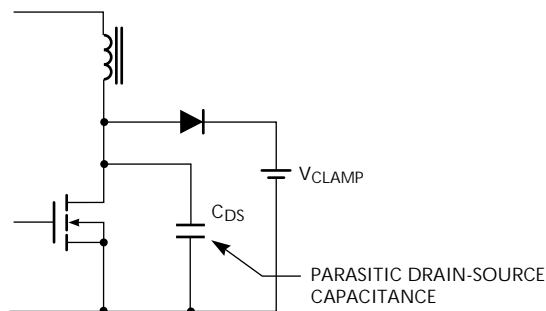


Figure 2. Typical switch stage of a switching power supply, with the parasitic drain-source capacitance shown explicitly.

The amount of power lost can be calculated by using the following formula

$$P = \frac{1}{2} C_{DS} V_{CLAMP}^2 f$$

As an example consider the following case  $C_{DS} = 500\text{pF}$ ,  $V = 380\text{ volts}$ ,  $f = 500\text{KHz}$  a circuit with these parameters results in a power loss of 18 watts. Therefore one can see the importance of capacitance  $C_{DS}$ .

In switching power supplies as we mentioned earlier it is often advantageous to use an external drain-source capacitance in the form of a snubber. This takes some of the burden of the switching loss from the switching device and puts it on the snubber circuits. The use of such capacitors further compounds the problem of capacitive discharge losses. If a way could be found to discharge the total drain-source capacitance non-dissipatively then that would represent a solution to the problem. Figure 3, shows this concept, for the time being we are not going to discuss the actual implementation of such a circuit. It is evident from the diagram that the switching loss can be reduced to zero if the voltage were also zero. From these diagrams it is evident that turn-on and turn-off power losses will be zero. Total switching times are in the order of 100nsec.

Zero Voltage Switching techniques represent such a solution. There are some limitations and shortcomings even to these techniques. When ZVS is accomplished through resonance of the voltage waveform then the design and analysis of such power supplies is more complicated. As a rule of thumb the operating drain currents are also higher than in PWM controlled power supplies.

To summarize, the ideal power supply would be the one that doesn't have operating frequency limitations because of switching losses, would be easy to design and manufacture and will be cost effective utilizing each one of its components to their fullest extent. In the next section we will discuss such a topology that has many of these desirable characteristics.

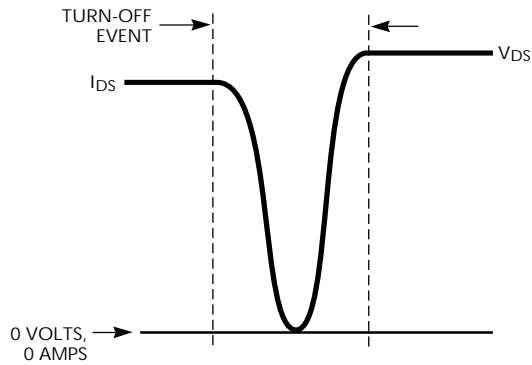


Figure 3a. Ideal turn-off waveforms of a ZVS switching element.

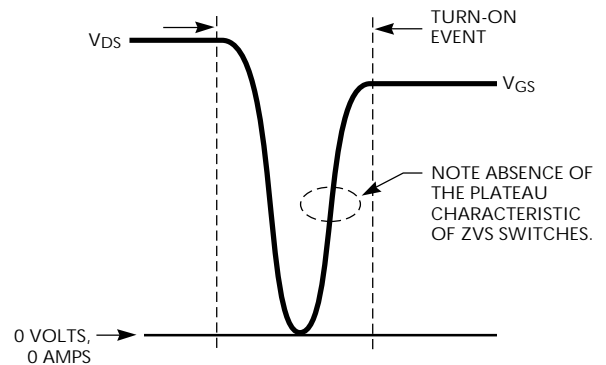


Figure 3b. Ideal turn-on waveforms of a ZVS switching element.

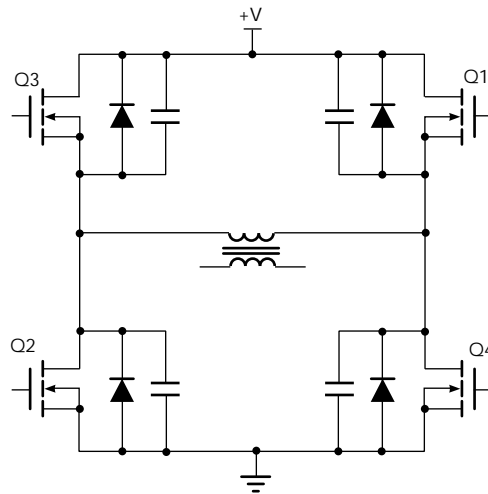


Figure 4. Typical H bridge power switch configuration as it is used in medium to high power switching power supplies.

## PHASE MODULATED PWM TOPOLOGY (PMPT)

Phase modulated PWM Topology although not a panacea has many of the favorable characteristics mentioned above. It is a promising topology for medium to high power systems. Basically it is a full bridge topology with appropriately coordinated gate drive waveforms for each one of the MOSFETs in the H bridge. Its operating waveforms are very close to ideal. Turn-on and turn-off switching losses are almost eliminated. Operating drain currents are almost equivalent to those of a regular full bridge PWM topology, thus it does not require the use of expensive large die area MOSFET switches. The only difference is how the two topologies handle their respective switching events.

The analysis and design of the power circuit of the PMPT topology is identical to that of the classical PWM topology. Having said that, there are special set of considerations associated with the design of a high frequency high power transformer used in the PMPT.

*The key idea behind the PMPT is that the voltage across the MOSFET is allowed to swing to “zero volts” just before the start of the next conduction cycle in the respective switches.*

Figure 4, shows a typical H bridge configuration, the diodes and the capacitors across the MOSFETs are the intrinsic parasitic components present in these components. Typical values for the capacitors range anywhere from 100pF to 500pF for the larger devices. The reverse recovery time of the body diodes are in the range of 100nsec. In the figure snubber circuitry has not been shown.

The power switch section of the PMPT is identical to the one shown in Figure 4. To achieve PMPT operation the switches must be driven differently. In the regular PWM topology, gate drive is applied to the two diagonal switches based on the required duty cycle, then there is a period during which all switches are OFF (deadtime) and then gate drive is applied to the opposing diagonal switches.

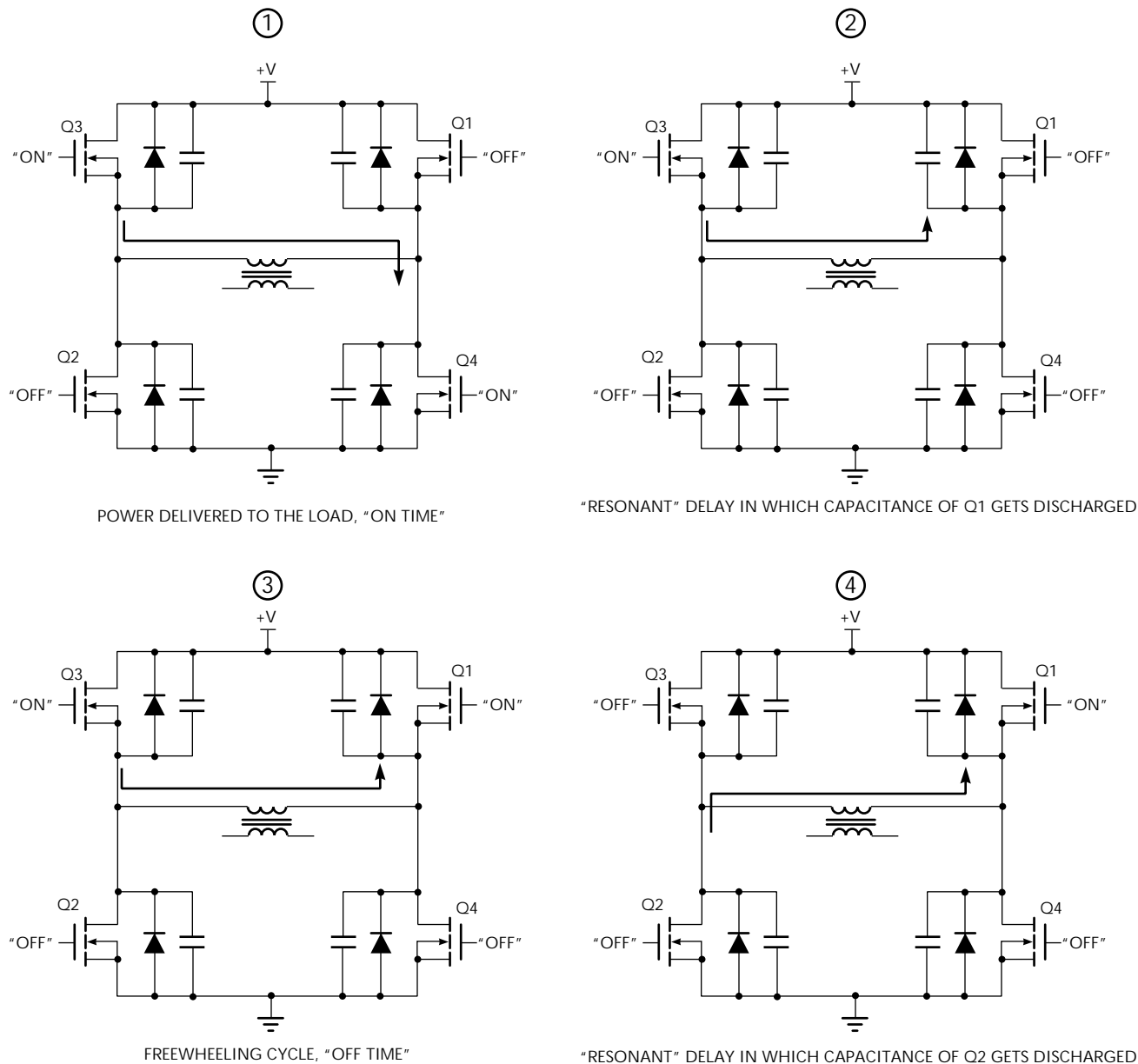


Figure 5a. PMPT power circuit cycles.

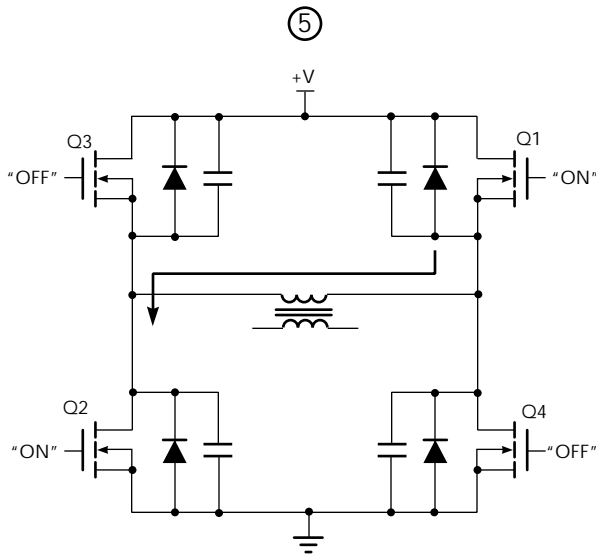
In the PMPT in order to accomplish ZVS, the leakage, and magnetizing inductances of the power transformer are utilized along with the drain-source capacitances of the power MOSFETs. The body diode of the MOSFETs also serves to clamp positive and negative going voltages. Thus the parasitic components of the MOSFETs are put to good use with this topology.

*Sometimes in order to further reduce the turn-off losses additional capacitance may be necessary across the drain-source of each MOSFET.*

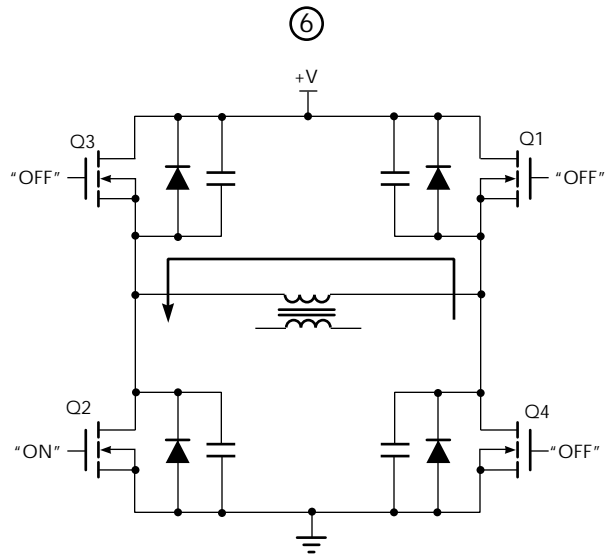
The operation of the PMPT is best understood by examining one full cycle of events in the power circuit. For the time being one can assume that the power transformer magnetizing and leakage inductances will behave as current sources. Figures 5a and 5b show the power stage of the PMPT through one complete cycle.

1. The two diagonal MOSFETs are conducting, power is delivered through the transformer to the load. The primary load current is flowing through the leakage inductance of the transformer. The total primary current is equal to the load current plus the increasing magnetizing current of the transformer. The magnetizing current is of importance here since when the output load is very light there is very little reflected load current to complete the ZVS action.

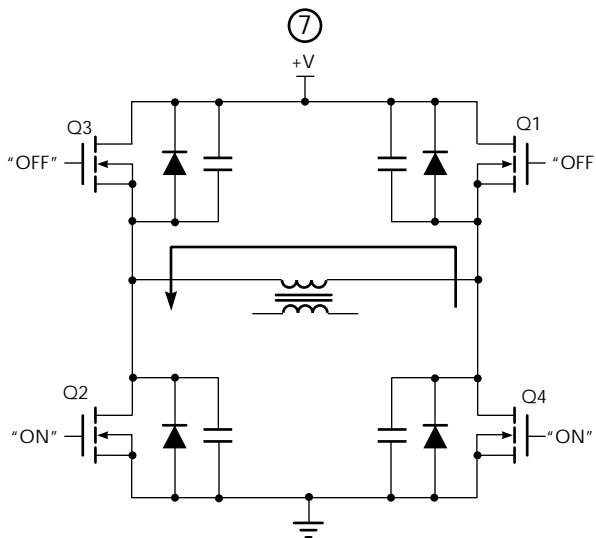
2. Q4 turns off, the capacitance across Q1 was charged to +V when Q4 was ON with the turning OFF of Q4 the current through the transformer inductances starts to charge the drain-source capacitance of Q4 while at the same time discharges the capacitance of Q1. This action continues until the body diode of Q1 turns ON to clamp the voltage across Q1 to approximately -0.7V. The current through the transformer is sustained in the upper half of the power circuit as shown in the figure of phase (2).



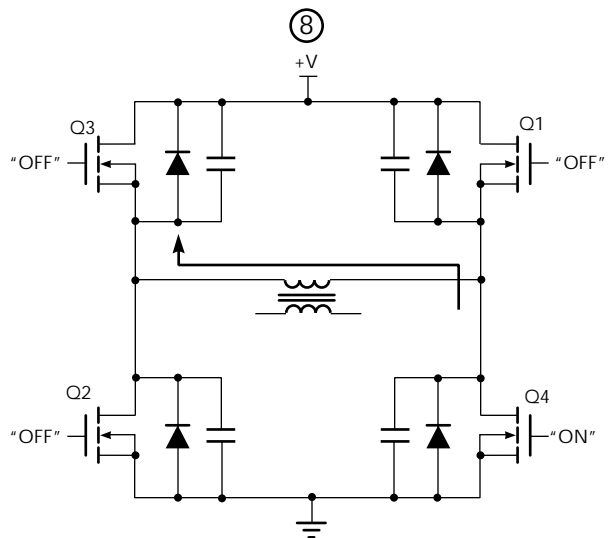
ZERO VOLTAGE SWITCHED "ON TIME." POWER DELIVERED TO THE LOAD.



"RESONANT" DELAY IN WHICH CAPACITANCE OF Q4 GETS DISCHARGED



FREEWHEELING CYCLE "OFF TIME"



"RESONANT" DELAY IN WHICH CAPACITANCE OF Q3 GETS DISCHARGED

Figure 5b. PMPT power circuit cycles.

3. When the voltage across Q1 reaches approximately "0 volts" Q1 turns ON. The time that is required for the capacitance of Q4 and Q1 to reach the desired voltage is programmed as delays in the gate drive waveforms of the controller. This delay is programmable with an external resistor for complete flexibility. The current in this phase is circulating through the conduction channels of Q3 and Q1.

4. Q3 turns off, the transformer current now starts to charge and discharge the capacitances of Q3 and Q2 respectively. It requires again a finite amount of time for the drain voltage of Q2 to reach "0 volts" this time is consistent with the programmed delay at the outputs of the controller. It is the presence of this delay that makes ZVS possible. When the voltage across Q2 reaches "0 volts" then Q2 will be turned ON with no voltage across it. Thus accomplishing our goal of non-dissipative turn ON switching.

5. With the complete discharge of its drain source capacitance Q2 now is ready to turn ON. Power is delivered to the load through the conducting path of Q1 and Q2 for an amount of time that is determined by the control circuit. The product of this time, times two, times the operating frequency of the oscillator gives the duty cycle of the converter as in regular PWM converters.

$$\text{Duty Cycle} = 2t_{\text{ON}}f$$

Thus the calculation of output voltages or of the required transformer turns ratio becomes a task that is quite similar to that of the regular PWM converters. The difference is that in regular PWM converters the magnetizing inductance is maximized in order to get the minimum amount of magnetizing current. In the PMPT magnetizing current has to be at certain level to facilitate ZVS when the reflected load current to the primary is insufficient to do so. This magnetizing current adds to the reflected load

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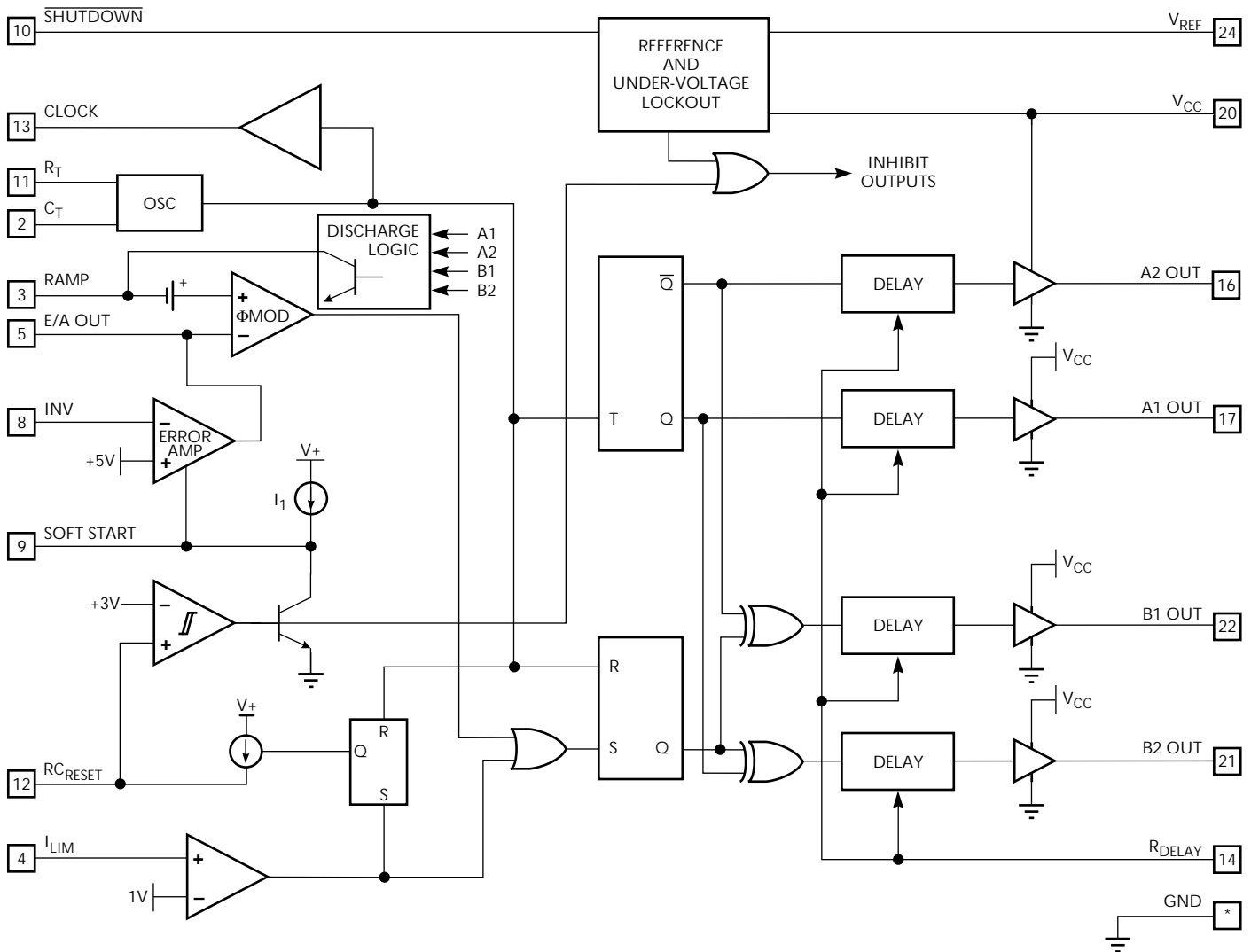
current thus requiring the use of a lower  $R_{DS}$  MOSFET. This is the penalty paid by using the PMPT. In any case the requirements are far less if conventional resonant technique were to be used.

6. Following the power transfer of the above diagonal pair, Q1 turns OFF. The voltage across Q4 starts to decrease, and when this voltage reaches "0 volts" the next phase starts.
7. In this phase Q4 turns on and the primary current circulates in the conduction channels of the lower pair.
8. Q2 turns OFF and the current starts to charge and discharge the capacitances of Q2 and Q3 respectively. When the voltage across Q3 has reached "0 volts" then Q3 turns ON non-dissipatively and the complete cycle repeats itself from phase (1).

## CONTROL CIRCUIT CONSIDERATIONS

The ML4818 PMPT controller has been designed to generate all the necessary timing and gate waveforms, and it contains logic circuitry for effective fault management that is of paramount importance in high power switching power supplies.

The control method involved instead of attempting to change the pulse width of the switches, changes the pulse width of the power pulse. Each of the switches operates under constant duty cycle that approaches 50%. In actuality the duty ratio is in the range of 40% to 45%. The remaining 5% to 10% of the time is being used for the ZVS action to take place. The above percentages may change with various operating frequencies. The effective maximum power pulse width can be much closer to 50%



\*PINS 1, 6, 7, 15, 18, 19 AND 23 ARE GND

Figure 6. Functional Block diagram of the ML4818.

for optimum performance at lower frequencies (for example at 100KHz). A demonstration board is available from Micro Linear that operates at about 500KHz. Probing this board is a very good way of learning about the various operating modes of this very important class of PWM topologies.

Lets now discuss how phase modulation is accomplished. Earlier we mentioned that each of the four switches in the power bridge circuit has its own gate drive waveform. That requires four individual gate drive signals to be generated by the control circuit. This is exactly what the ML4818 does. The controller has four outputs that can directly drive the four MOSFETs. Figure 6 shows the internal block diagram of this controller.

In order to fully understand the control mechanism, we will look into the heart of the controller. Figure 7 shows the phase modulator core of the controller. All fault and supervisory circuitry has been left out. Also both of the complementary outputs and all driver and delay blocks have been left out for further simplicity. By examining

how the other two outputs behave, one is able to grasp the basic operating principles of the phase modulator.

As can be seen from Figure 7, the core of the circuit is quite simple. Assuming that the two comparators are inactive for the time being the only stimulus that the circuit receives is from the clock pulse. Under this assumption the circuit reduces to the one shown in Figure 8.

From Figure 8, clearly if the set input of FFB is always logic "0" then the "Q" output of FFB will be reset or logic "0". From the operation of the exclusive OR gate then the "B" output will be equal to the inverted output of FFA i.e., outputs A and B will be 180 degrees out of phase from each other. Figure 9, shows the relevant waveforms.

If now we assume that a periodic stimulus is present at the set Input "S" of FFB occurring at some instance other than the clock pulse instance then the resulting waveforms will be different as is evident by examining Figures 8 and 9. The resulting timing diagram is shown in Figure 10.

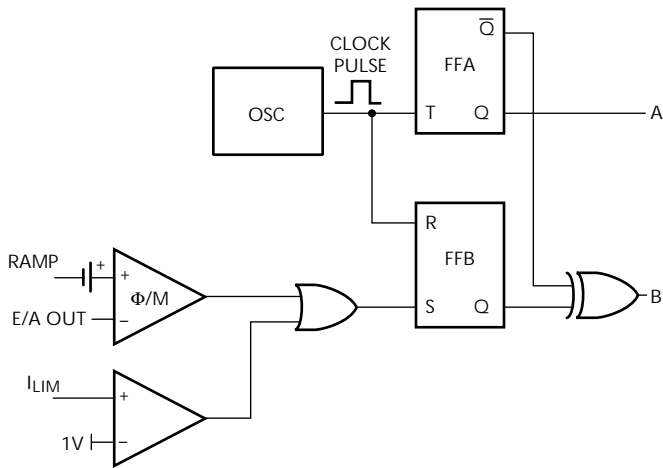


Figure 7. Phase modulator of the ML4818.

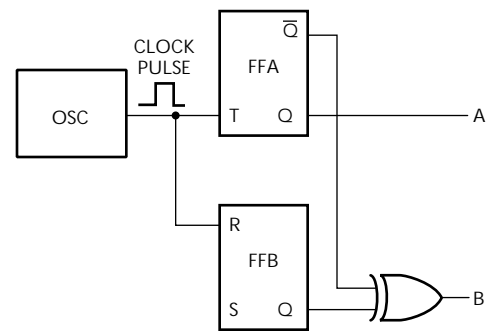


Figure 8. Phase modulator control logic.

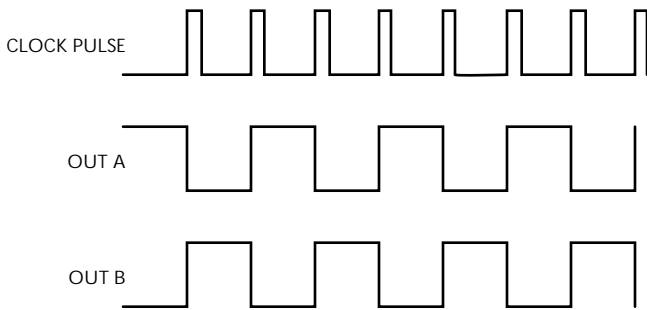


Figure 9. Timing waveforms of the basic phase modulator at the absence of stimulus other than the clock pulse.

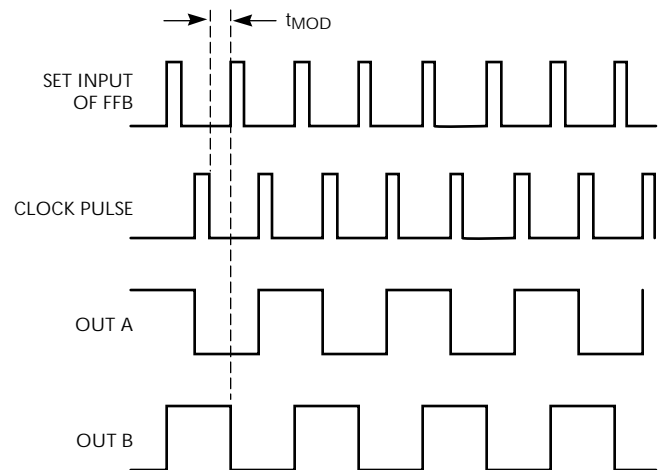


Figure 10. Resulting timing waveforms when there is a periodic stimulus at input "S" of FFB with period T equal to the period of the clock pulse.

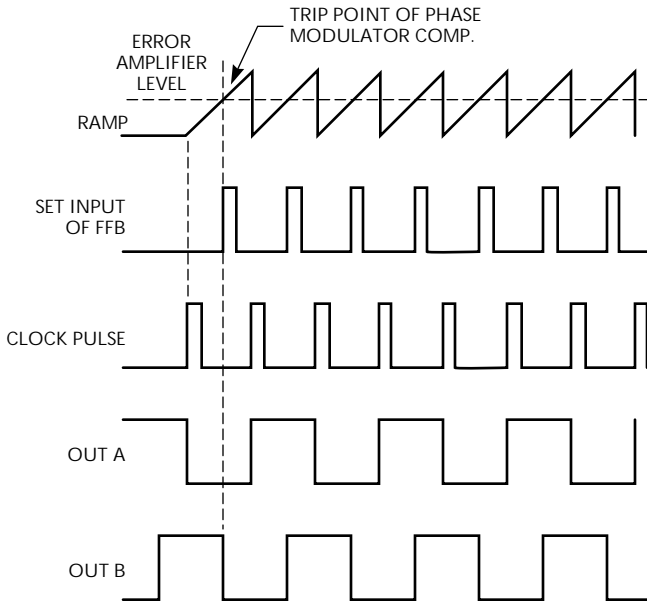


Figure 11. Generation of the set pulse for FFB. Ramp shape may be different in actual application.

Output "A" is free toggling whenever the clock pulse is present, whereas output "B" is the exclusive OR'ed output that is the result of outputs FFA,  $\bar{Q}$  and FFB. The exclusive OR gate here functions as a controlled inverter. The other two outputs of Figure 6, behave in similar way with the only difference that they are 180 degrees out of phase with the ones described above.

By controlling time  $t_{MOD}$  then we are able to control the phase shift between outputs "A" and "B". The set input pulse for FFB is normally generated by either the phase modulator comparator of Figure 12, or by the current limit comparator. As in normal PWM regulators one input of the phase modulator comparator is the output of the error amplifier which sets the trip level and the other input is either a voltage ramp or the sensed primary (or secondary) current waveform of the power circuit. Figure 11, shows the generation of the set pulse and the resulting timing waveforms. When the output of the error amplifier changes then the trip level changes thus it is possible to continuously control time  $t_{MOD}$  by changing the trip level. In switching power supplies it is also necessary to limit the power pulse width whenever the primary load current exceeds certain predetermined value. The second comparator in Figure 7, serves that purpose. Thus the output of the phase comparator and of the current limit comparator are logic OR'ed to produce the set pulse for FFB. Figure 12, shows the complete logic diagram of the phase modulator with four outputs labeled A1, A2, B1, and B2 respectively.

The timing waveforms for all outputs can be derived from the above diagram. Figure 13, shows the relationship of the outputs with respect to each other.

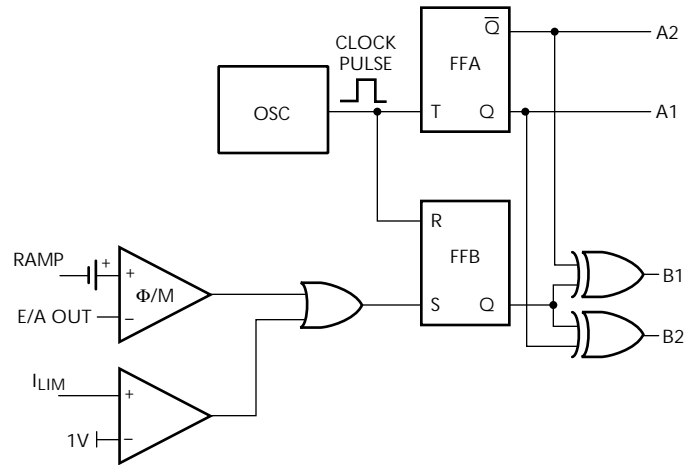


Figure 12. Complete logic diagram of the phase modulator with all four outputs shown.

## DELAY OF THE GATE DRIVE WAVEFORM

So far we saw how controllable phase shifted outputs could be generated. We also saw that in order to have ZVS in the bridge circuit in the transition phase between conduction of the opposing legs, one of the MOSFETs is ON and the remaining are OFF. It is during this time that the drain source capacitance of the device next to turn ON is discharged to "zero volts". In the traditional H-bridge either two of the devices are ON or all of them are OFF.

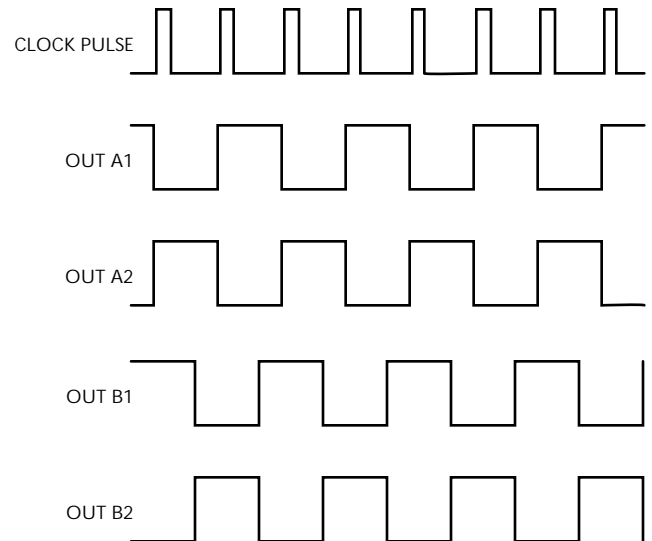


Figure 13. Timing diagram showing the waveform present on all four outputs of the phase controller.

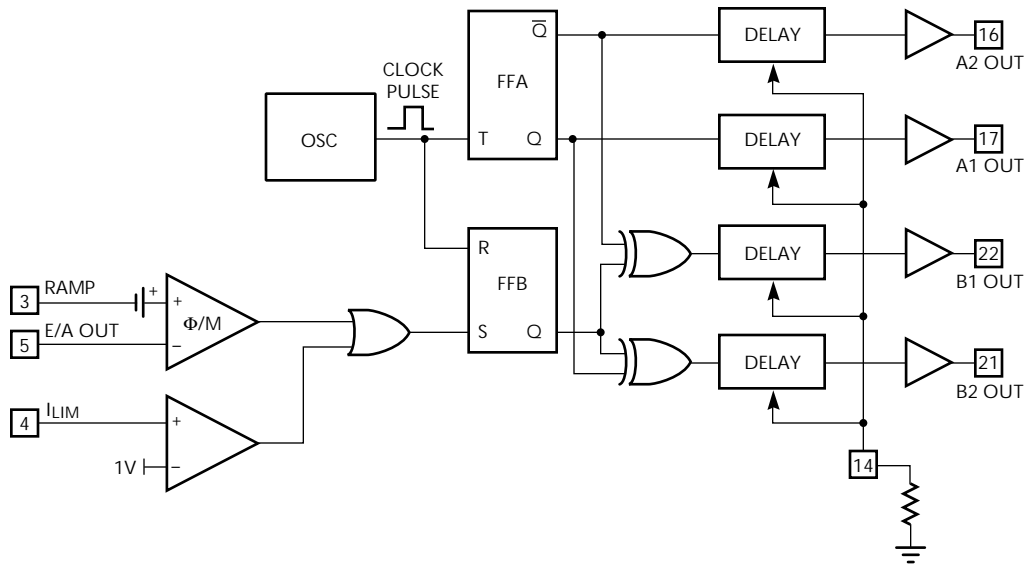


Figure 14. Phase modulator with delay and output driver blocks shown.

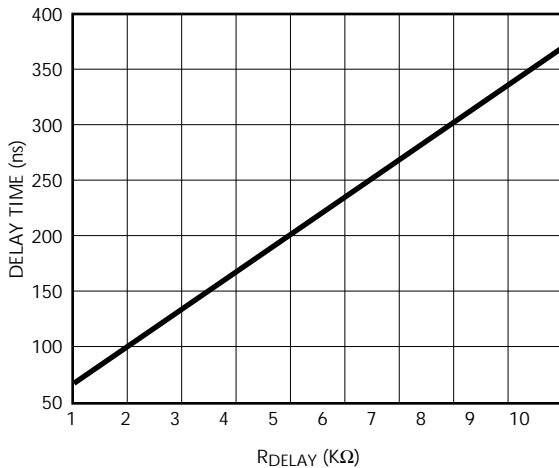


Figure 15. Chart for the determination of the external delay resistor.

In order to get this transition period it is necessary to modify the gate drive waveforms slightly. The modification consists of adding a predetermined amount of delay to the leading edge of the gate drive waveforms. Figure 14, shows the phase modulator along with the delay and output driver blocks. The delay blocks contain all the necessary electronics for the generation of the delay with the use of a single external resistor. The timing capacitor is integrated into the part. The value of the delay resistor  $R_{DELAY}$  can be found by using the chart of Figure 15, or it can be calculated by using the formula below

$$R_{DELAY} = \frac{DELAY(ns) - 33.34}{33.33} k\Omega$$

The individual gate drive waveforms are restricted to less than 50%. The resulting waveforms are shown in Figure 16. The shaded area in the leading edges shows the reduction in the pulse width. Note that the delays are only present at the leading edges of the waveforms. Hence the less than 50%

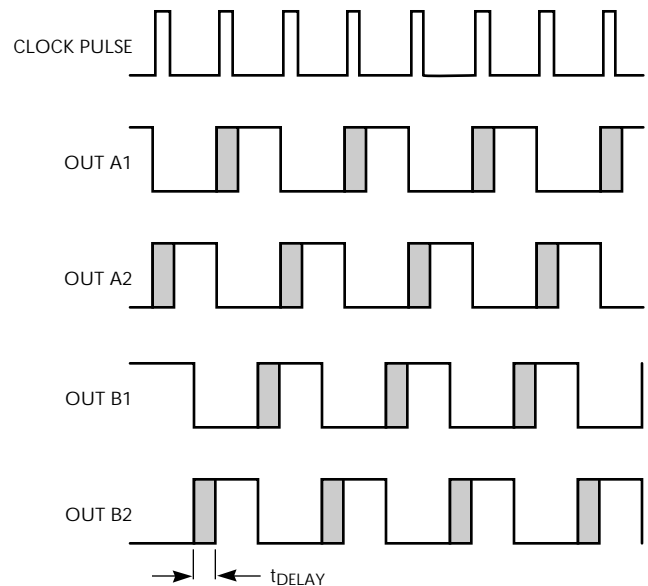


Figure 16. Leading edge delay of the drive waveforms necessary for ZVS operation.

duty cycle. Because all the drive signals have this delay complementary waveform symmetry is preserved. Although the delay time can be adjusted using an external resistor, it should be kept in mind that resulting actual delays in the power circuit may differ, this will be due to slew of the drive waveforms, also it requires a finite time to charge and discharge the gate capacitances of the MOSFETs.

The amount of time that is required to complete ZVS will vary as the load current reflected to the primary varies. The power transformer magnetizing inductance has to be able to develop enough current during "ON time" for ZVS to complete its cycle. That will require careful design of the power transformer. In most cases the transformer will have to be gapped. A side effect of the gapping will be the stabilization of the magnetizing inductance.

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The idealized power transfer cycles of the PMPT are shown in Figure 17. Power transfer takes place during the hatched periods. The width of these periods depends on the phase relationship between the "A" and "B" outputs. A good way to observe the phase modulation action is watch the oscilloscope traces of "A1" and "B1" outputs.

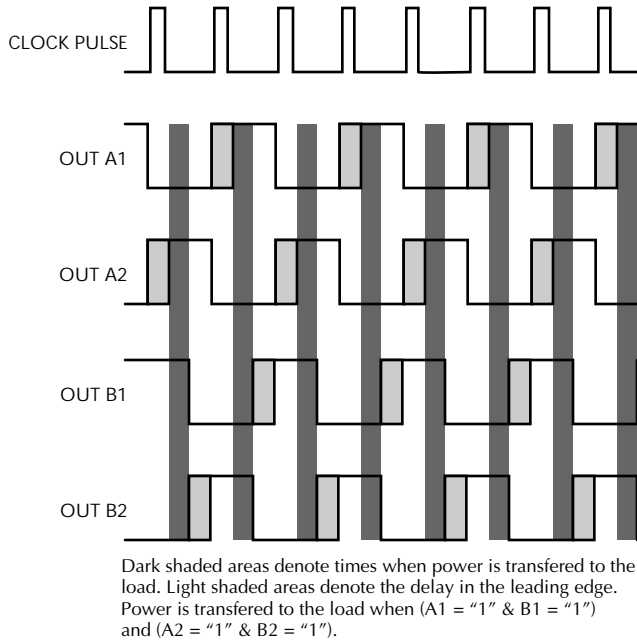


Figure 17. Power transfer cycles of the PMPT.

## DESIGNING FOR ZERO VOLTAGE SWITCHING

So far we saw that it is possible to do non-dissipative switching. The ML4818 power supply controller with its operational flexibility is able to provide all the necessary waveforms needed for such power supply. The most important thing left to be done is the design of the power transformer. Zero Voltage Switching properties greatly depend on this component.

Figure 18, shows the simplified equivalent model of a typical power transformer. The model is indeed very simple, actual transformers are very difficult to model due to the presence of primary and secondary effects such as saturation and inter-winding capacitances.

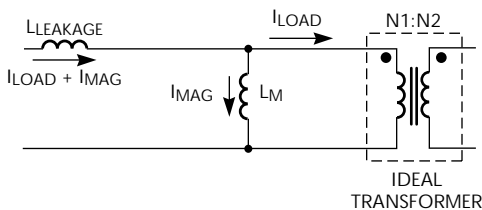


Figure 18. Simplified model of a real transformer.

It is obvious from Figure 18, that the current that will flow through the MOSFETs will be the sum of both the reflected secondary current which we call the load current and of the current that builds up in the magnetizing inductance of the transformer.

The load current is a function of the output load and can change anywhere from zero to its full rating as it reflects to the primary. The magnetizing current on the other hand is a function of the ON time and of the primary applied voltage. The output filter inductor where the load current flows through is normally very large. For all practical purposes the reflected current of the primary can be assumed constant during the intervals of interest.

$$I_{MAG} = \frac{V_{IN} t_{ON}}{L_M}$$

It is also important to remember that inductors can be approximated as current sources. With all this in mind lets now look into what happens when a power MOSFET switches OFF. Figure 19, shows one leg of the bridge circuit with the parasitic drain source capacitances. Assuming that the lower device was conducting current just prior to turning off the following events may happen.

If the gate drive waveform is fast enough and drops to zero volts before the drain source capacitance can charge to any significant voltage then the turn off event will be non-dissipative. This is the principle also with snubbers, where a large amount of external capacitance diverts the current from the channel for non-dissipative switching. Where the PMPT excels is that just before turn ON the energy stored in the snubber or drain source capacitances of the MOSFETs is returned back to the source as we saw earlier. This way there is not a penalty for using additional snubber capacitance. And since the turn ON is at zero voltage the switching event is lossless even at very high frequencies i.e., 500KHz and above.

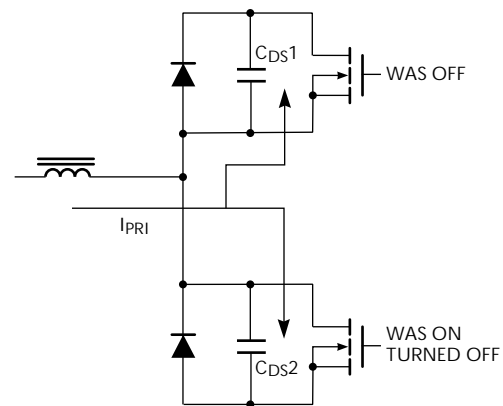


Figure 19. MOSFET switching in PMPT, and charge and discharge of the drain source capacitances.

In Figure 19, in order to discharge the drain source capacitances there needs to be a certain amount of current stored in the inductances of the transformer. Since the total charging current is the sum of the load currents and the magnetizing current, whenever the load current is low the charging has to be done by the current that the magnetizing inductance was charged. Hence the importance of the magnetizing inductance.

One can get quite complicated in trying to calculate the required amount magnetizing inductance necessary for ZVS. But the following simple procedure could be followed with some experimentation to get familiar with the technique.

The required maximum duty cycle is the first parameter to consider. Along with the delay that will be introduced by the delay circuit of the ML4818, in high frequency conversion the effective duty cycle will be reduced by the charging effect of the leakage inductance. Here we will assume that the reduction of the duty cycle by the charging of the leakage inductance is negligible (not true in most of the cases).

Lets assume that the required duty cycle results in a delay time  $t_D$ . In other words the time available to complete the charging of the drain source capacitance is  $t_D$ . *The charging configuration of the bridge circuit changes depending on its state just prior to ZVS. In Figure 19, the bridge circuit was delivering power to the secondary, so it was in a power transfer cycle just prior to the next ZVS. Under this condition the drain source capacitances will be charged linearly by a current equal to*

$$I_{PRI} = I_{LOAD} + I_{MAG}$$

This is not the worst case. The worst case happens after the above there is a period of freewheeling of the current before the next device turns ON with ZVS. This corresponds to phases (3) and (4) in Figure 5a. During this period the output diodes effectively short the transformer and the only inductance in the circuit is the leakage inductance and carries a current slightly less than at the end of the power transfer cycle. Therefore all the calculations are based on this case.

*During phases (2) and (3) the capacitances charge linearly with the reflected load current. During phases (3) and (4) the capacitances resonate with the leakage inductance and charge in a resonant fashion. The worst case is when the load current is very close to zero. Under that condition the freewheeling current in the leakage inductance is equal to the magnetizing current at the end of the power transfer cycle.*

The assumption we are going to make is that the delay time represents one quarter of the resonant cycle determined by the leakage inductance and twice the drain source capacitance of the MOSFETs, since there are two MOSFETs per side.

The procedure for calculating the necessary amount of the leakage and magnetizing inductances is shown below. An important note here is that in most of the cases the leakage inductance will be determined by the actual transformer construction and it will be a given. In that case the equation below could be used first to calculate the required amount of the delay time.

1. Calculate the required amount of either delay or leakage inductance value when one of them is the given value

$$\frac{1}{4t_D} = \frac{1}{T} = \frac{1}{2\pi\sqrt{2C_{DS}L_{LEAKAGE}}} \Rightarrow$$

$$L_{LEAKAGE} = \frac{2}{C_{DS}} \left( \frac{t_D}{\pi} \right)^2$$

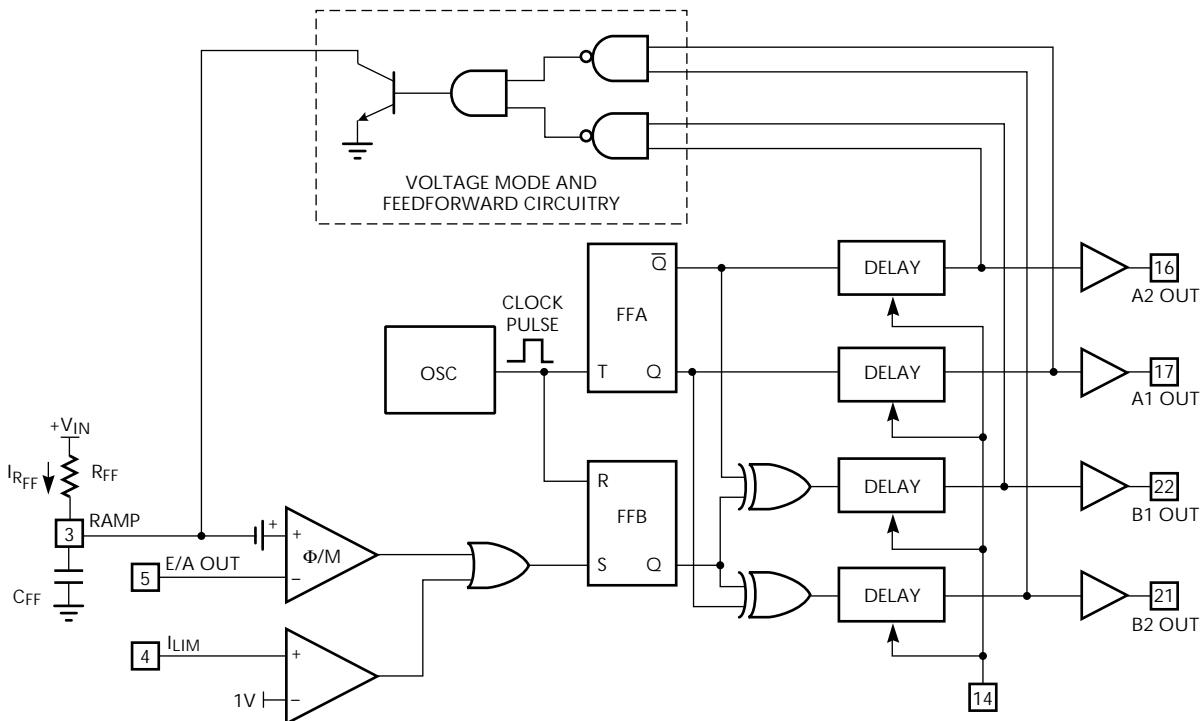


Figure 20. Voltage mode and feed-forward circuitry of the ML4818.

or

$$t_D = \pi \sqrt{\frac{C_{DS} L_{LEAKAGE}}{2}}$$

2. Calculate the minimum current for ZVS from the energy required to reach  $V_{IN(max)}$ . Note that twice the energy necessary to swing one leg of the bridge is required to be stored by the leakage inductance. This is because we have two ZVS actions during one complete power transfer cycle.

$$\frac{1}{2} L_{LEAKAGE} I_{MAG(min)}^2 = 4 \left( \frac{1}{2} C_{DS} V_{IN(max)}^2 \right) \Rightarrow$$

$$L_{LEAKAGE} I_{MAG(min)}^2 = 4 C_{DS} V_{IN(max)}^2 \Rightarrow$$

$$I_{MAG(min)} = \sqrt{\frac{4 C_{DS} V_{IN(max)}^2}{L_{LEAKAGE}}}$$

3. Calculate the value of  $L_{MAG}$ .

$$L_{MAG} = \frac{V_{IN} t_{ON}}{I_{MAG(min)}}$$

Example: Lets suppose that the following are given

$$L_{LEAKAGE} = 15\mu H$$

$$C_{DS} = 225pF$$

$$V_{IN(max)} = 370Volts$$

$$t_{ON}(@V_{IN(max)}) = 1\mu sec$$

The calculations for the above example are as follows:

$$T_D = 3.14 \sqrt{\frac{(225pF)(15\mu H)}{2}} = 129nsec$$

$$I_{MAG(min)} = \sqrt{\frac{4(225pF)(370V)^2}{15\mu H}} = 2.86A$$

$$L_{MAG} = \frac{(370V)(1\mu sec)}{2.86A} = 95.85\mu H$$

The value of the magnetizing inductance found above is somewhat low. This is because we made the assumption that there will be ZVS down to very light loads. If we do not allow the output load to go to very light loads or if we are willing to live with NZVS (Near Zero Voltage Switching) then the resulting magnetizing inductor values will be higher resulting in lower conduction losses. The value of magnetizing inductance that was chosen for the typical PMPT power supply of Figure 23, was 400 $\mu$ H, the value of the leakage inductance was approximately 15 $\mu$ H.

## MORE ABOUT THE ML4818 CONTROLLER, VOLTAGE OR CURRENT MODE OPERATION

The ML4818 controller is able to control a PMPT converter operating either voltage mode or current mode. It contains special logic circuitry for that purpose. That same circuitry allows for voltage feed-forward in voltage mode operation. Figure 20, shows the logic circuit internal to the IC that enables the above.

Pin #3 is pulled to ground at the end of the power cycle and is kept at ground until the start of the next power transfer cycle. Thus the discharge of the feed-forward capacitor is enabled. An important note here is that the PMPT operating in voltage mode required the internal logic of Figure 20. It is not possible to operate voltage mode by only connecting pin #3 to the oscillator ramp. This is unlike conventional PWM regulators.

Feed-forward voltage mode operation provides automatic line correction without the need for the voltage control loop to change the duty cycle. The correction takes place within a single cycle. The current through resistor  $R_{FF}$  is proportional to input voltage therefore the charging time of the  $C_{FF}$  capacitor is proportional to input line voltage and consequently the time that it takes to reach the threshold set by the error amplifier.

$$I_{R_{FF}} = \frac{V_{IN}}{R_{FF}}$$

$$t_{ON} = \frac{V_{E/A} C_{FF}}{I_{R_{FF}}} = \frac{V_{E/A(max)} C_{FF} R_{FF}}{V_{IN(min)}}$$

The necessary values for any given application can be calculated using the above equations which can be solved for any of the unknown values. The resulting ramp will affect the open loop gain of the voltage control loop. The open loop gain will be independent of the variations in input voltage. The open loop gain for the voltage mode controlled case can be calculated by using the following.

$$G_{o.l.} = \frac{C_{FF} R_{FF} f_{OSC}}{N}$$

where  $N$  = Primary to secondary turns ratio

$f_{OSC}$  = oscillator frequency

$G_{o.l.}$  = open loop voltage gain

For the circuit in Figure 23, the open loop voltage gain was calculated to be 7 or 16.9db, below the corner frequency of the output filter. In this case the corner frequency is 4.1KHz.

## A TYPICAL PMPT POWER SUPPLY

Figure 23, shows a typical off-line PMPT supply, as it can be seen from the schematic diagram only a handful of components are required to build a fully functional power supply. Specifications for this supply are shown in Table 1.

The power supply was not optimized for any particular application. It is important to note that higher efficiencies

can be obtained by using lower loss magnetic materials and lower ON resistance MOSFETs.

The controller in this design is located at the primary side. The voltage feedback is accomplished with the use of an optocoupler. The current transfer ratio for this optocoupler is almost linear for a limited operating range, this enabled the use as it is shown in Figure 23. For more realistic applications an error amplifier at the secondary would probably be required. If an auxiliary supply is available then the controller itself can be situated in the secondary. Demonstration board that implements this power supply is available from Micro Linear Corp., it is a useful tool in gaining familiarity with this topology.

The control loop design for the voltage mode version of a PMPT supply is identical to that of a regular full bridge PWM converter. For simplicity in this case the loop is stabilized relying on the ESR of the output capacitor. The feedback components are calculated to give enough margin for loop stability.

The gate drive for the four MOSFETs is accomplished by using two drive transformers (T2 and T3). There are two secondary windings on each transformer to be able to drive the two MOSFETs in each leg of the bridge Figure 21, shows this configuration. The primary of the transformers connect to outputs A1, A2 and B1, B2 through a DC coupling capacitor to prevent drive core saturation under abnormal conditions. The windings of the transformers are trifilarly wound to minimize leakage inductances. A toroid of 0.5" outside diameter with 10 turns for each windings seem to

function fairly well. The wires should be insulated to provide isolation.

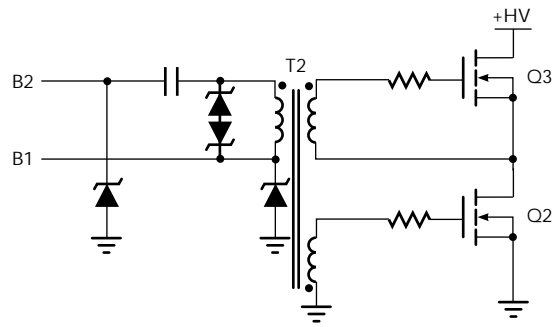


Figure 21. Gate drive scheme for fail-safe operation.

The power circuit consists of a DC blocking capacitor in series with the power transformer to prevent core saturation under unbalanced and abnormal conditions. The current transformer in series senses the current for cycle by cycle current limit. If the current limit persists then capacitor C8 charges to 3V triggering an internal comparator and shutting down the power supply. The resistor connected across C8 helps to discharge this capacitor and the power supply tries to soft start.

For high power applications where large size MOSFETs are used it may be necessary to use external gate drivers

Table 1.

Input Voltage Range	90VAC to 140VAC or 180VAC to 260VAC
Output Voltage	15V adjustable
Output Voltage Adjustment Range	12.6V to 20V (@ 120VAC and I <sub>out</sub> =13A)
Output Current	13.3A
Line Regulation (90VAC to 140VAC)	<30mV
Load Regulation (10% to 100% @ 20VAC)	<300mV
Current limit set to approximately	15A
Output Power	200W
Efficiency at full load and 120VAC	82%
Output Voltage Ripple	250mV (without additional filtering)
Voltage ramp time at turn on (0V to 15V)	<8msec
Oscillator Frequency	500KHz
Average power under short circuit	<10W
Short Circuit Capability	Indefinite
Short Circuit Protection Method	Hiccups

## Typical PMPT Power Supply Parts List

PART#	VALUE
<b>Resistors</b>	
R1, R2	240K, 1/4W
R3	82K, 2W
R4	39, 1/4W
R5, R20	1K, 1/4W
R9, R10, R11, R12	5.1, 1/4W
R6	4.3K, 1/4W
R7	240K, 1/4W
R8	7.5K, 1/4W
R13	510, 1/4W
R16	1K, 1/4W
R14	1K, 1/4W, POT
R15	100K, 1/4W
R17	330K, 1/4W
R19	100K, 1/4W
R21	5.1K, 1/4W
<b>Capacitors</b>	
C1, C2	680 $\mu$ F, 200V ELECTROLYTIC
C3	200 $\mu$ F, 25V, ELECTROLYTIC
C4	0.1 $\mu$ F, CER.
C5	680pF, PRECISION
C6	470pF, CER.
C7, C10, C15, C12, C16	1 $\mu$ F, CER
C8	56nF, CER
C9	0.33 $\mu$ F, 630V, POLYPROPYLENE
C11	100 $\mu$ F, 25V, ELECTROLYTIC
C14	0.01 $\mu$ F, 1KV, CER.
C18	1000pF, CER.
C20	220pF, CER.
C22	120pF, CER
C21	470pF, CER.
C23, C24	10nF, 1KV

to divert the power dissipation from the ML4818 controller to the external drivers. The drivers can be simple NPN-PNP pairs Figure 22, shows such a configuration.

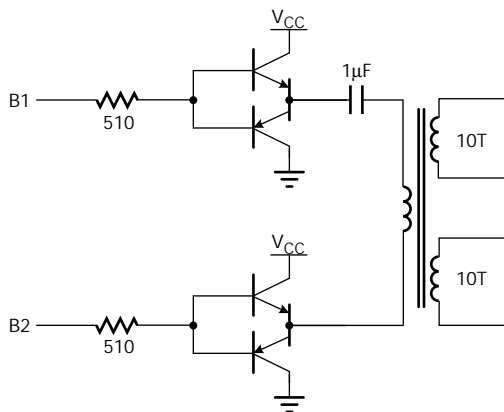


Figure 22. External gate drivers using NPN-PNP pairs.

PART#	VALUE
<b>Diodes</b>	
D1, D2	MUR150
D3, D4, D5, D6	1N5406, 3A, 600V
D9, D10, D11, D12	1N4148
D13	MBR3045PT, 30A, 45V, SCHOTTKY
D14, D15, D7, D8	1N5818, SCHOTTKY
D16, D17, D18, D19	1N5248, 18V ZENER
<b>MOSFETs</b>	
Q1, Q2, Q3, Q4	IRF840
<b>IC's</b>	
IC1	ML4818, PHASE-MOD. IC
OP1	MOC8102, OPTOCOUPLER
<b>Inductors</b>	
L1	200 $\mu$ H, 0.3A FILTER CHOKE
L2	15 $\mu$ H, LITZ WIRE, 15A FILTER CHOKE
<b>Transformers</b>	
T1	45T/2X4T/2X4T, Lmag = 400 $\mu$ H OBTAINED BY GAPPING, PRIMARY AND SECONDARIES ARE LITZ WIRE, Lleakage = 15 $\mu$ H, POT CORE, HIGH FREQUENCY MATERIAL
T2, T3	10T/10T/10T, GATE DRIVE TRANSFORMER, WOUND TRIFILAR ON 0.5" O.D. TOROID WITH INSULATED WIRE
T4	1T/80T, SAME CORE AS ABOVE, 80T IS AWG #28 MAGNET WIRE
<b>Fuses</b>	
F1	5A, 250V FUSE



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